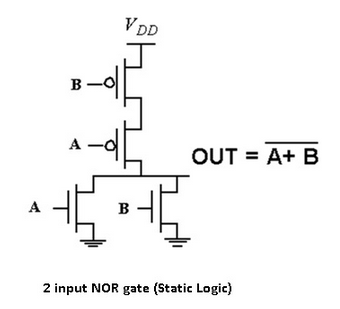
Experiment No. 05

**Layout of 2-input NOR gate**

**OBJECTIVE:** To simulate the Layout of 2-input NOR gate

**SOFTWARE**: Electric VLSI , LT Spice

**THEORY:** A 2-input NOR gate is shown in the figure below. The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.

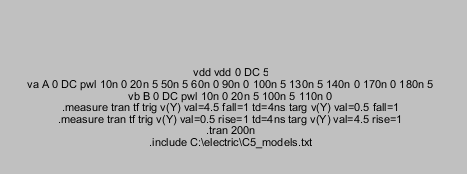
****The truth table of the NOR logic gate given in the below table.

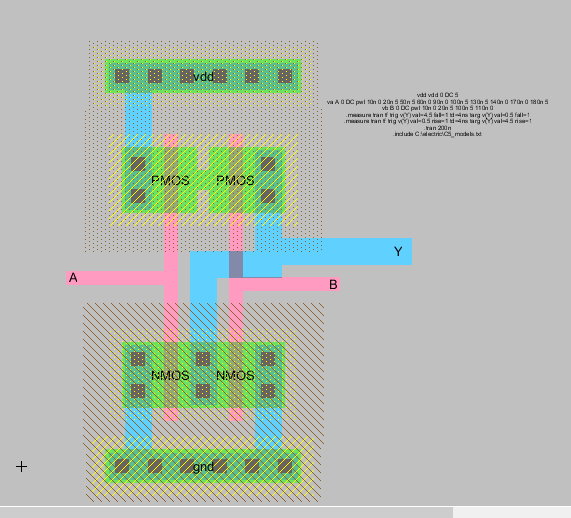
|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Y** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

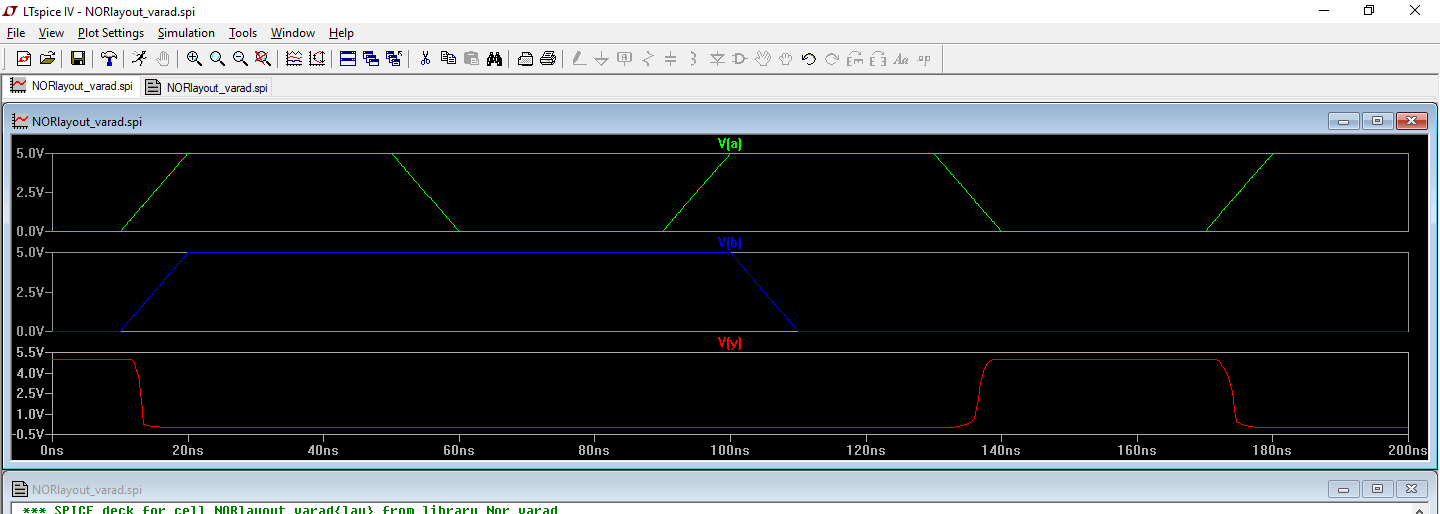
**PROCEDURE:**

1. Open Electric VLSI.
2. In **Files** Menu---click on **new** **library**---Give name to library.
3. In **Edit** Menu---click on **New Cell**---give name to cell---Select view as –schematic.
4. Go to **Components**---Select each required component----do connections.
5. In **Tools** menu---go to **Simulation(spice)**---**Set Spice model**. Select text Spice model and edit it to PMOS or NMOS according to the device.
6. **Create export**s as— A, B (for inputs) and Y (for output).
7. Write Spice code---by clicking on **Misc** in **components** and click on **spice code**.
8. Save library.
9. Simulate the schematic --- in **Tools** menu ----go to **Simulation(spice)**--- click on **Write Spice deck**.
10. LT Spice window gets opened. There Right click on the black window---click on **add trace**.
11. To see fall and rise time--- in **Edit** menu ---click on **SPICE error log**.

**OUTPUT:**







**CONCLUSION:**

Designing and Simulation of the layout of the 2 input NOR Gate using cmos implementation in electric vlsi was performed successfully. The output of NOR was plotted in ltspice and was verified.

**Name: Varad Uttam Patil**

**Roll no: 120A2036**

**Batch :- A3**